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HIS FORM IS BASED ON PTO/SB/30 (08-00)

REQUEST FOR

CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.

See The American Inventors Protection Act of 1999 (AIPA).

09/891,905
06/28/200
Gwan-hyeob Koh
2811
S. Gebremariam
5649-873

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application.

NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 13.53(d) (PTO/SB/29) instead of an RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and Provisional Application Practice, Final Rule, 65 Fed. Reg. 50092 (Aug. 16, 2000); Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat. Office 47 (Apr. 11, 2000), which was established RCF practice.

established RCE pri	actice.				
1. Submission re	quired under 37 C.F.R. § 1.114	4			
(Any u	sider the amendment(s)/reply u nentered amendment(s) referred to above w sider the arguments in the Appe	rill be entered).			
b. 🛛 Enclose	d	01/31/2003 EARE	 GAY1 000	000096 500220 09891905	
ii. 🔲 Affid	ndment Accompanying RCE avit(s)/Declaration(s) mation Disclosure Statement (I r	01 FC:1801	750.0		
2. Miscellaneous					
a period	sion of action on the above-ider of months. (Period of				
3. Fees The	RCE fee under 37 C.F.R. § 1.17(e) is require	ed by 37 C.F.R. § 1.114	when the	RCE is filed.	
a. ⊠ The Dir ¹Deposit Ac i. ⊠ RCE	ector is hereby authorized to choount No. 50-0220. fee (\$750) required under 37 (nsion of time fee (37 C.F.R. § § or	harge the followi	ng fees	, or credit any overpaym	ents, to
iii. ☐ Othe	r	3 1.130 and 1.17	,	טרני	EB SEC
b.	n the amount of \$	er	closed	45	1- 8 EE
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Name (Print/Type)	SIGNATURE OF APPLICAN Robert N. Crouse	I, ATTORNET,		ation No. (Attomey/Agent)	44.635
Signature	Robert is: Clouse		Date	January 23, 2003	44,033
	Muly			dandary 20, 2000	
CERTIFICATE OF MAILING OR TRANSMISSION I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Box RCE, Washington, DC 20231, or facsimile transmitted to the U.S. Patent and Trademark Office on:					
Name (Print/Type)	Susan E. Freedman				
Signature	Susan E. A.	uduan	<u>Dat</u> e	January 23, 2003	



Attorney Docket No.: 5649-873

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Koh et al.

Filed: June 26, 2001

Serial No.: 09/891,905

Group Art Unit: 2811

Examiner: Samuel A. Gebremariam

Confirmation No.:1424

For: METHODS OF FORMING INTEGRATED CIRCUITS USING MASKS TO

PROVIDE ION IMPLANTATION SHIELDING TO PORTIONS OF

SUBSTRATE ADJACENT TO AN ISOLATION REGION THEREIN

January 23, 2003

BOX RCE Commissioner for Patents Washington, DC 20231

AMENDMENT ACCOMPANYING RCE

Sir:

This Amendment is responsive to the Final Official Action of October 23, 2002 and the Advisory Action of January 3, 2003. Pursuant to the rules for amendments under 37 C.F.R. § 1.121, the claims have been amended herein using the rewritten claims format. The present amendment also includes a section entitled "VERSION WITH MARKINGS TO SHOW CHANGES MADE" attached hereto.

In the Claims:

Please replace Claims 1 and 21 with the following like numbered claims:

Sub !

(Twice Amended) A method of forming a channel region between isolation regions of an integrated circuit substrate, the method comprising:

forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween, the exposed portion of the substrate comprising a first portion where a gate electrode will be subsequently formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions;